CERTIFICATE OF MAILING BY FIRST CLASS MAIL (37 CFR 1.8) Applicant(s): **Tamal Bose et al.**			Docket No. **51764/2**
Serial No. **10/615,004**	Filing Date **July 8, 2003**	Examiner	Group Art Unit **2631**

Invention:

INFINITE IMPULSE RESPONSE MULTIPLIERLESS DIGITAL FILTER ARCHITECTURE

I hereby certify that this **Information Disclosure Statement; PTO-1449 with copies of articles; postcard.**
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is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

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John R. Thompson
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Tamal Bose et al. Confirmation No. 8129

Application No. 10/615,004

Filed: July 8, 2003

For: **INFINITE IMPULSE RESPONSE MULTIPLIERLESS DIGITAL FILTER ARCHITECTURE**

Group Art Unit: 2631

Examiner:

Date: February 27, 2004

INFORMATION DISCLOSURE STATEMENT

TO THE COMMISSIONER FOR PATENTS:

1. Pursuant to the duty of disclosure, documents listed on the accompanying Form PTO-1449 (or equivalent) are presented for the Examiner's consideration.

☒ Copies of listed documents are enclosed. (37 CFR § 1.98(a))

☐ Copies of listed U.S. patent documents are omitted because this application was filed after June 30, 2003 and is, thus, subject to image file wrapper processing. Copies of listed foreign patent documents and non-patent literature are enclosed.

☐ Copies of the documents listed on sheet(s) _____ of Form PTO-1449 (or equivalent) are omitted because (1) they are already of record in U.S. Patent Application No. _____, filed _____, on which this application relies for an earlier filing date under 35 U.S.C. § 120; and (2) any information disclosure statement filed in the prosecution of Application No. _____, complies with 37 CFR §§ 1.98(a) through (c). (37 C.F.R. § 1.98(d))

2. ☐ The Examiner's attention is directed to the enclosed copy of copending U.S. Patent Application No. _____, filed _____, for _____, which is cited in this application.

3. This information disclosure statement is being submitted (check box a., b., or c.):

a. ☒ Within three months of the filing date of a national application or entry of the national stage in an international application; or before the mailing of a first Office action on the merits; or before the mailing of a first Office action after the filing of a request for continued examination under 37 CFR 1.114. (No statement under 37 CFR 1.97(e) is required.); or

b. ☐ After the period set forth in paragraph 3a, but before the mailing date of either a final action, a notice of allowance, or an action that otherwise closes prosecution in the application. (Check box i. or ii.)

i. ☐ A $180.00 information disclosure statement submission fee set forth in 37 CFR 1.17(p) is enclosed, or

ii. ☐ A statement specified by 37 CFR 1.97(e) is set forth below; or

c. ☐ After the mailing date of a final action or notice of allowance and on or before payment of the issue fee. A statement specified by 37 CFR 1.97(e) is set forth below. Enclosed is a $180.00 information disclosure statement processing fee set forth in 37 CFR 1.17(p).

4. If a statement specified by 37 CFR 1.97(e) is required, the attorney or agent signing below hereby states that:

☐ each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement; or

☐ no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement.

5. ☐ A concise explanation of the relevance of each document not in the English language and/or selected documents in the English language is set forth below.

Respectfully submitted,

By _____
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FORM PTO-1449 (REV. 7-80) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 51764/2	APPLICATION NO. 10/615,004
INFORMATION DISCLOSURE CITATION	APPLICANT – Tamal Bose et al.	
Title: **INFINITE IMPULSE RESPONSE MULTIPLIERLESS DIGITAL FILTER ARCHITECTURE**	FILING DATE- July 8, 2003	

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformation with MPEP609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICA-TION DATE	COUNTRY / PATENT OFFICE	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
								☐

OTHER DOCUMENTS (Including Author, Title, Date, Relevant Pages, Place of Publication , etc.)

	1	Yu et al., "New Natural Selection Process and Chromosome Encoding for the Design of Multiplierless Lattice QMF Using Genetic Algorithm," 2001 IEEE, pgs. 1273-1276.
	2	Sriranganathan et al., "Design of 2-D Multiplierless FIR Filters Using Genetic Algorithms," Genetic Algorithms in Engineering Systems: Innovations and Applications 12-14 September 1995, Conference Publication No. 414, © IEE, 1995, pgs. 282-286.
	3	Bhattacharya et al., "Multiplierless Implementation of Recursive Digital Filters Using a Class of Low Sensitivity Structures," International Symposium on Signal Processing and its Applications (ISSPA), Kuala Lumpur, Malaysia, 13-16 August, 2001, Organized by the Dept. of Microelectronics and Computer Engineering, UTM, Malaysia and Signal Processing Research Centre, QUT, Australia, 2001 IEEE, pgs. 611-614.
	4	Lee et al., "GA-based design of multiplierless 2-D state-space digital filters with low roundoff noise," IEE Proc.-Circuits Devices Syst., Vol. 145, No. 2, April 1998, pgs. 118-124.
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	8	Cemes et al., "Genetic approach to design of multiplierless FIR filters," ELECTRONICS LETTERS, 25th November 1993, Vol. 29, No. 24, pgs. 2090-2091.
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	11	Oh et al., "Design of Discrete Coefficient FIR and IIR Digital Filters with Prefilter-Equalizer Structure Using Linear Programming," IEEE Transactions on Circuits and Systems—II: Analog and Digital Signal Processing, Vol. 47, No. 6, June 2000, pgs. 562-565.
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	21	Lian, "FPGA Implementation of High Speed Multiplierless Frequency Response Masking FIR Filters," Electrical Engineering Department, National University of Singapore, 10 Kent Ridge Crescent, Singapore 119260, 2000 IEEE, pgs. 317-325.

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	22	Lutovac et al., "Approximate Linear Phase Multiplierless IIR Halfband Filter," IEEE Transactions on Signal Processing Letters, Vol. 7, No. 3, March 2000, pgs. 52-53.
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